Capacitor Charger Controller

FEATURES

- Charges Any Size Capacitor
- Easily Adjustable Output Voltage
- Drives High Current NMOS FETs
- Primary-Side Sense—No Output Voltage Divider Necessary
- Wide Input Range: 3V to 24V
- Drives Gate to V_{CC} – 2V
- Available in 10-Lead MS Package

APPLICATIONS

- Emergency Warning Beacons
- Professional Photoflash Systems
- Security/Inventory Control Systems
- High Voltage Power Supply
- Electric Fences
- Detonators

DESCRIPTION

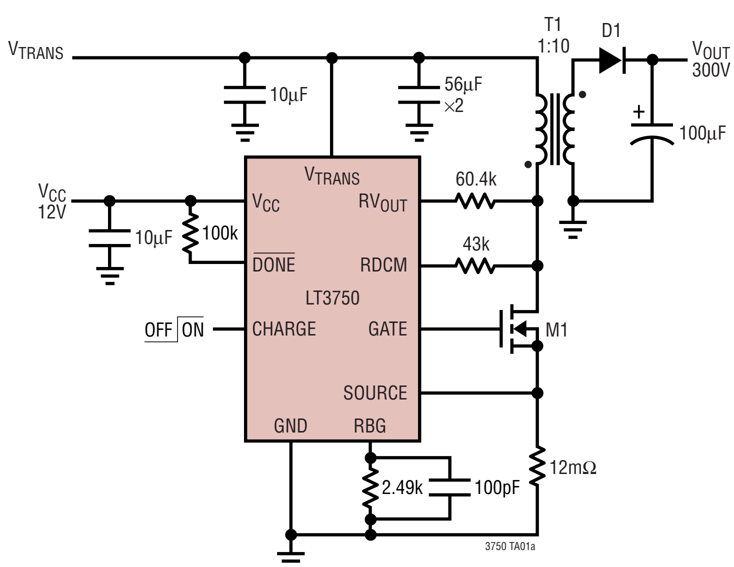
The LT®3750 is a flyback converter designed to rapidly charge large capacitors to a user-adjustable target voltage. A patented boundary mode control scheme* minimizes transition losses and reduces transformer size. The transformer turns ratio and two external resistors easily adjust the output voltage.* A low 78mV current sense accurately limits peak switch current and also helps to maximize efficiency. With a wide input voltage range, the LT3750 can operate from a variety of power sources. A typical application can charge a 100µF capacitor to 300V in less than 300ms.

The CHARGE pin gives full control of the LT3750 to the user. The DONE pin indicates when the capacitor has reached its programmed value and the part has stopped charging.

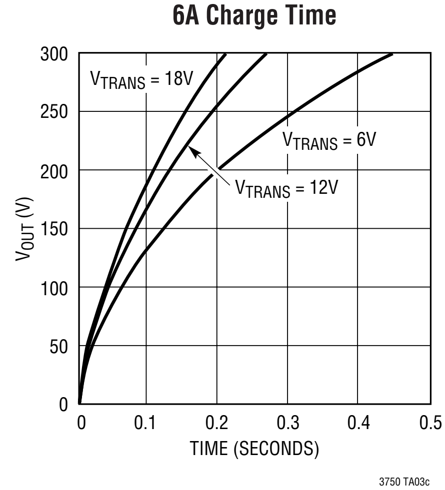
*Protected by U.S. Patents, including 6518733, 6636021.

TYPICAL APPLICATION

300V, 6A Capacitor Charger



6A Charge Time

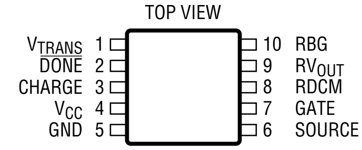


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{CC}, V_{TRANS}, GATE, $\overline{DONE}$, CHARGE 24V
RBG 1.5V
SOURCE 1V
Current into RDCM Pin .... ±1mA
Current into RV_{OUT} Pin .... ±1mA
Current into $\overline{DONE}$ Pin .... ±1mA
Operating Temperature Range (Note 2) .. –40°C to 85°C
Storage Temperature Range .... –65°C to 150°C

PACKAGE/ORDER INFORMATION



MS PACKAGE
10-LEAD PLASTIC MSOP
$T_{JMAX} = 125°C, \theta_{JA} = 120°C/W$

ORDER PART NUMBER	MS PART MARKING
LT3750EMS	LTBQD

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are $T_A = 25°C$. $V_{CC} = V_{TRANS} = 5V$ unless otherwise specified.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum V_{CC}		●		2.8	3	V
Minimum V_{TRANS}		●		2.5	3	V
V_{CC} Quiescent Current	Not Switching, CHARGE = 5V Not Switching, CHARGE = 0V			1.6	2.5 1	mA µA
V_{TRANS} Quiescent Current	Not Switching, CHARGE = 5V Not Switching, CHARGE = 0V			140	250 1	µA µA
CHARGE Pin Current	CHARGE = 24V CHARGE = 5V CHARGE = 0V			24 19	 1	µA µA µA
CHARGE Pin Enable Voltage		●		0.87	1.1	V
CHARGE Pin Disable Voltage		●	0.2	0.6		V
Minimum CHARGE Pin Low Time	High→Low→High				20	µs
V_{OUT} Comparator Trip Voltage	Measured RBG Pin	●	1.215	1.24	1.265	V
V_{OUT} Comparator Overdrive	1µs Pulse Width, Measured on RBG Pin			30		mV
RBG Pin Bias Current	RBG = 1.2V			70	500	nA
DCM Comparator Trip Voltage	Measured as $V_{DRAIN} – V_{TRANS}$, R_{DCM} = 43k (Note 3)	●	5	36	80	mV
Current Limit Comparator Trip Voltage		●	68	78	88	mV
$\overline{DONE}$ Output Signal High	100kΩ to 5V		4.9	5		V
$\overline{DONE}$ Output Signal Low	100kΩ to 5V			0.1	0.2	V
$\overline{DONE}$ Pin Leakage Current	$\overline{DONE}$ = 2.5V				0.2	µA
NMOS Minimum On Time				0.6		µs
GATE Rise Time				50		ns
GATE High Voltage	C_{GATE} = 1nF, V_{CC} = 5V C_{GATE} = 1nF, V_{CC} = 24V		3 22	3.8 22.6	4.5 23.5	V V
GATE Turn Off Propagation Delay	C_{GATE} = 1nF			100		ns

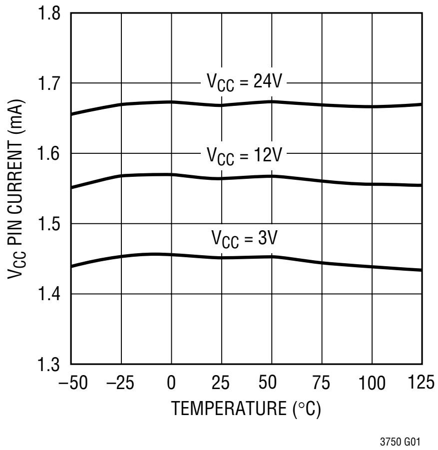
Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT3750E is guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

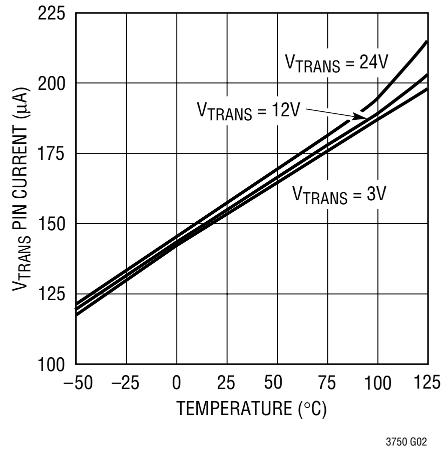
Note 3: Refer to Block Diagram for V_{DRAIN} definition.

TYPICAL PERFORMANCE CHARACTERISTICS

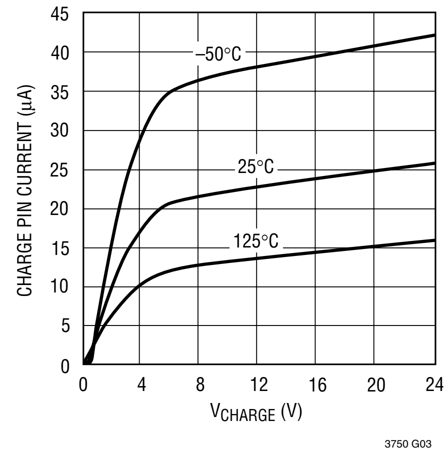
V_{CC} Pin Current



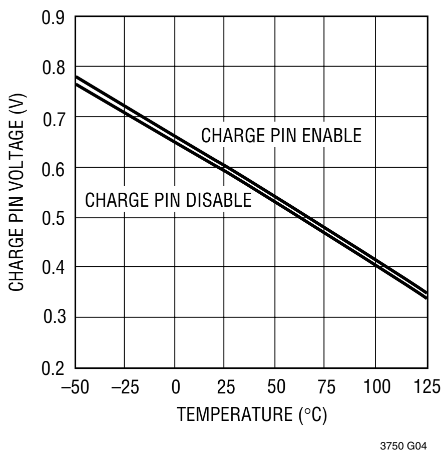
V_{TRANS} Pin Current



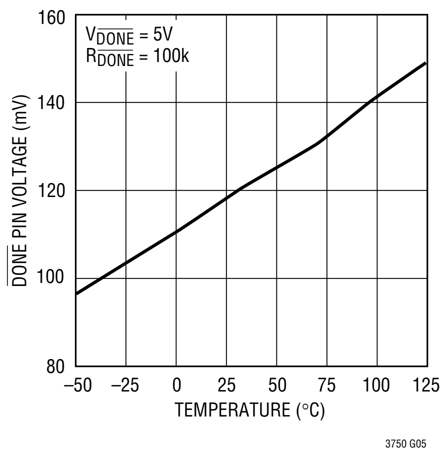
CHARGE Pin Current



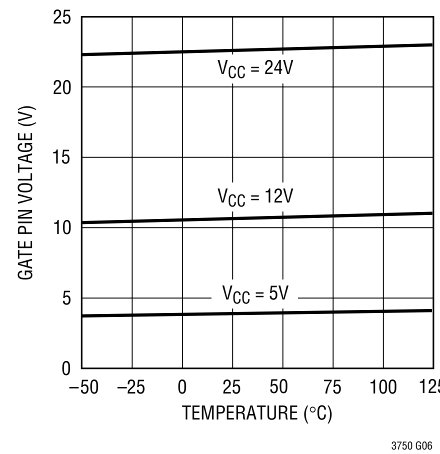
CHARGE Pin Enable/Disable Voltage



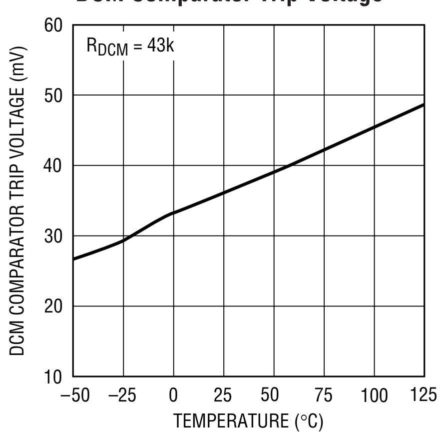
$\overline{\text{DONE}}$ Output Signal Low



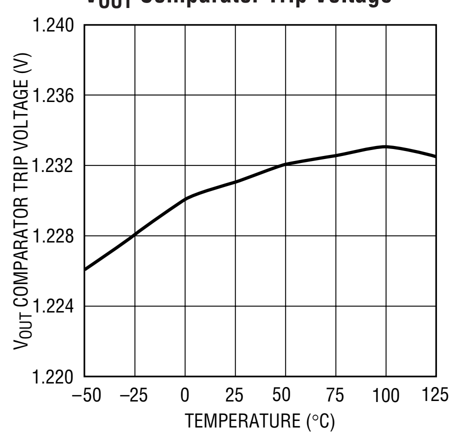
GATE High Voltage



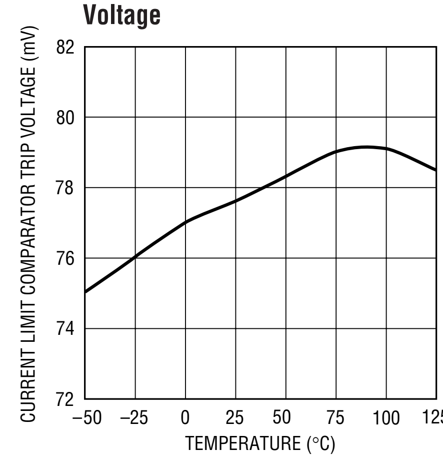
DCM Comparator Trip Voltage



V_{OUT} Comparator Trip Voltage



Current Limit Comparator Trip Voltage



PIN FUNCTIONS

V_{TRANS} (Pin 1): Transformer Supply Pin. Powers the primary coil of the transformer as well as internal circuitry that performs boundary mode detection. Bypass at the pin with a 1μF to 10μF capacitor. Bypass the primary winding of the transformer with a large capacitor.

$\overline{\text{DONE}}$ (Pin 2): Open Collector Indication Pin. When target output voltage is reached, an NPN transistor turns on. Requires a pull-up resistor or current source. Any fault conditions such as thermal shutdown or undervoltage lockout will also turn on the NPN.

CHARGE (Pin 3): Charge Pin. Initiates a new charge cycle when brought high or discontinues charging and puts part into shutdown when low. To properly enable the device, a step input with a minimum ramp rate of 1V/μs is required. Drive to 1.1V or higher to enable the device; drive below 0.2V to disable the device.

V_{CC} (Pin 4): Input Supply Pin. Bypass locally with a ceramic capacitor. A 1μF to 10μF ceramic capacitor should be sufficient for most applications.

GND (Pin 5): Ground Pin. Connect directly to local ground plane.

SOURCE (Pin 6): Source Pin. Senses NMOS drain current. Connect NMOS source terminal and current sense resistor to this pin. The current limit is 78mV/R_{SENSE}.

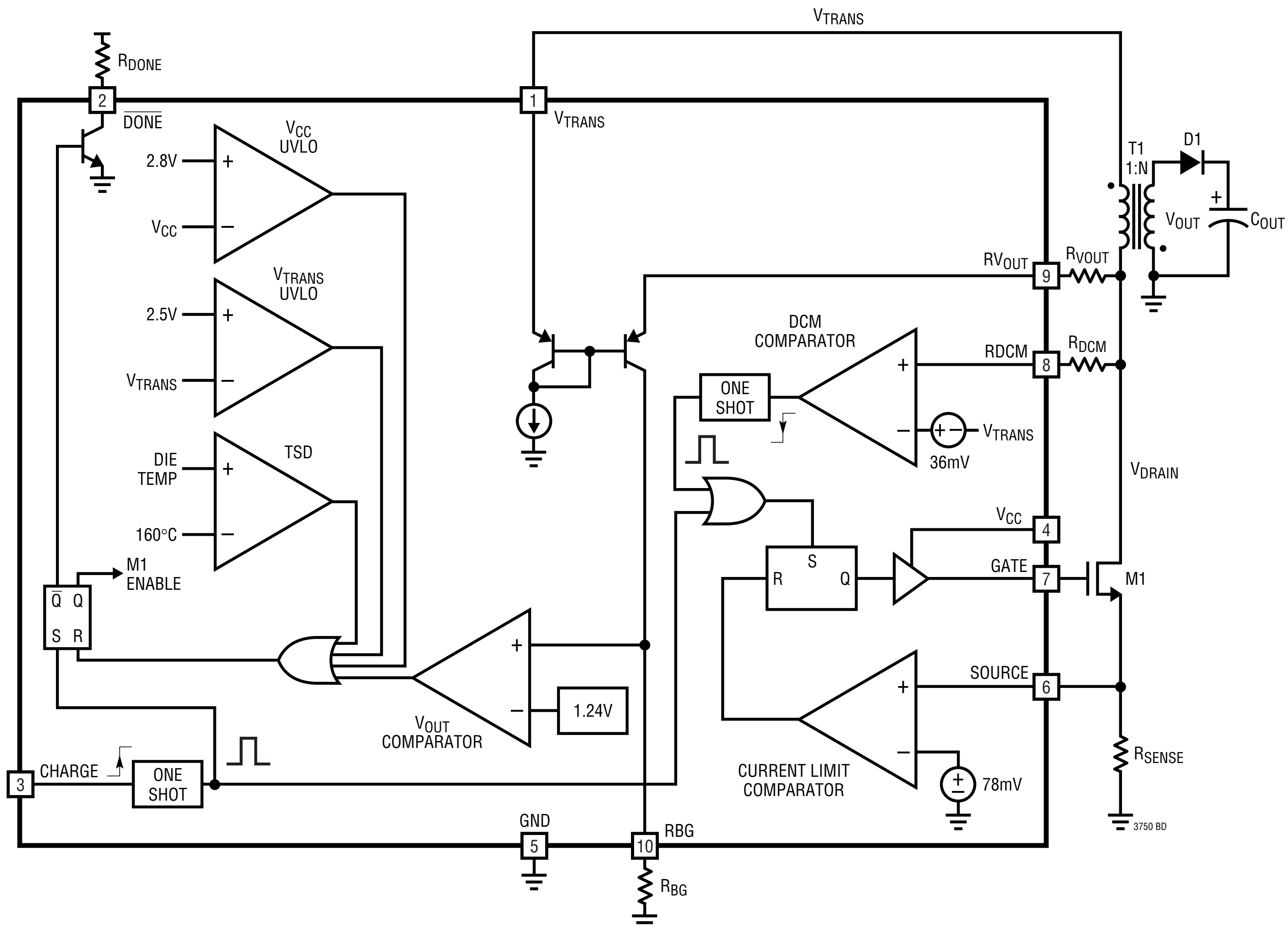
GATE (Pin 7): Gate Pin. Connect NMOS gate terminal to this pin. Internal gate driver will drive voltage to within V_{CC} – 2V during each switching cycle.

RDCM (Pin 8): Discontinuous Mode Sense Pin. Senses when current in transformer has decayed to zero and initiates a new charge cycle if output voltage target has not been reached. Place a resistor between this pin and the drain of the NMOS. A good choice is a 43k, 5% resistor.

RV_{OUT} (Pin 9): Output Voltage VI Converter Pin. Develops a current proportional to output capacitor voltage. Connect a resistor between this pin and the drain of the NMOS.

RBG (Pin 10): Output Voltage Sense Pin. Senses the voltage across the RBG resistor, which is proportional to the current flowing into the R_{VOUT} pin. When voltage equals 1.24V, charging is disabled and $\overline{\text{DONE}}$ pin goes low. Connect a resistor (2.5k or less is recommended) from this pin to GND. A 2.49k, 1% resistor is a good choice.

BLOCK DIAGRAM

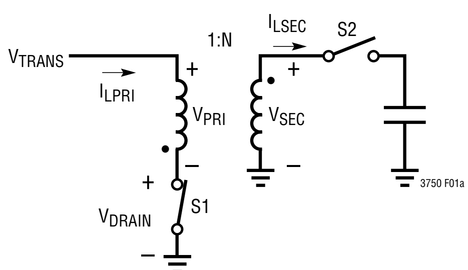


OPERATION

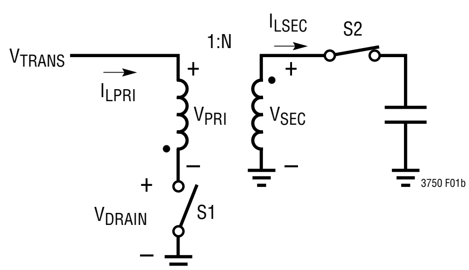
The LT3750 is designed to charge capacitors quickly and efficiently. Operation can be best understood by referring to Figures 1 and 2. Operation proceeds in four phases: 1. Start-up, 2. Primary-side charging, 3. Secondary energy transfer, 4. Discontinuous mode sensing.

1. Start-Up

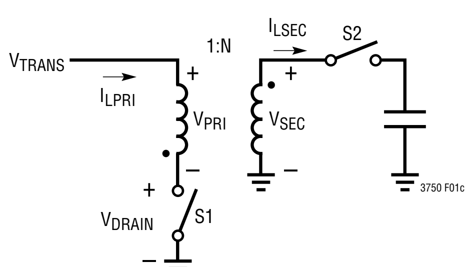
Start-up occurs for approximately 20µs after the charge pin is raised high. During this phase, a one-shot enables the master latch and turns on the NMOS. The master latch will remain in the set state until the target output voltage is reached or a fault condition resets it.



(1a) Equivalent Circuit During Primary-Side Charging



(1b) Equivalent Circuit During Secondary Energy Transfer and Output Detection



(1c) Equivalent Circuit During Discontinuous Mode Detection

Figure 1. Equivalent Circuits

2. Primary Side Charging

When the NMOS on latch is set, the gate driver rapidly charges the gate pin to $V_{CC} - 2V$. The external NMOS turns on forcing $V_{TRANS} - V_{DS(ON)}$ across the primary winding. Consequently, current in the primary coil rises linearly at

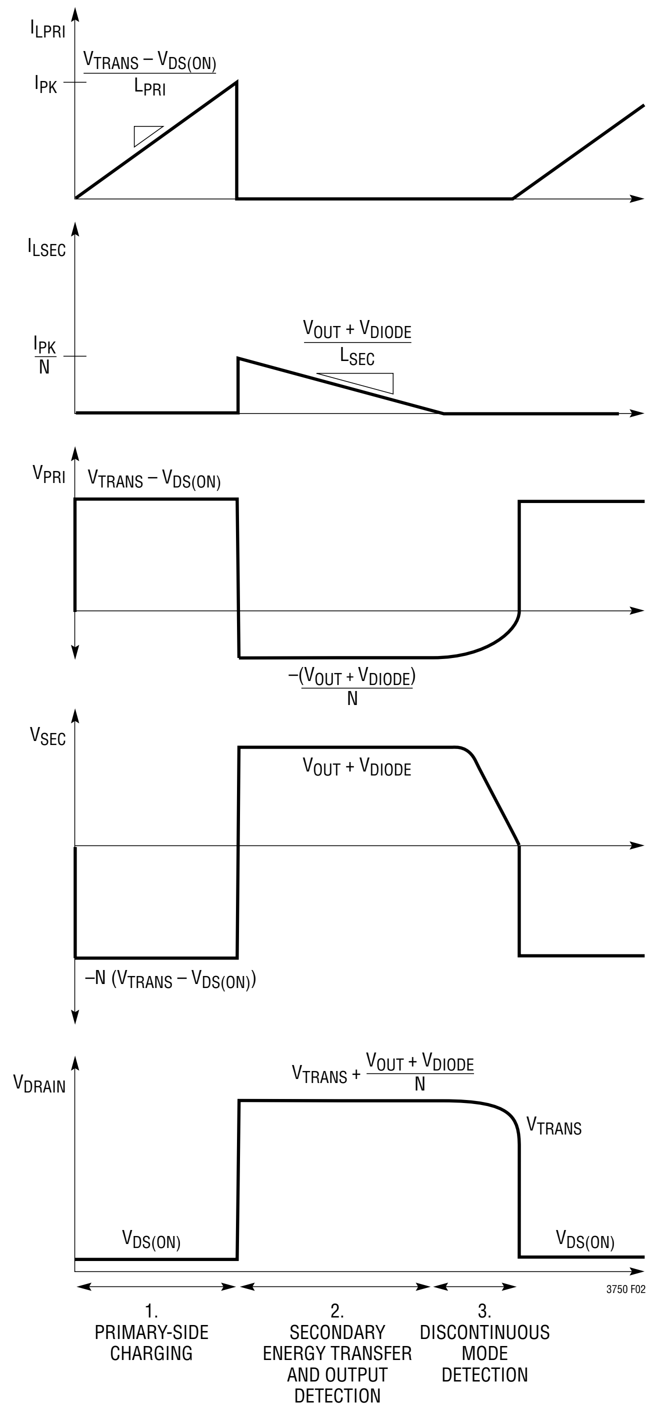


Figure 2. Idealized Charging Waveforms

OPERATION

a rate (V_{TRANS} – $V_{DS(ON)}$)/L_{PRI}. The input voltage is mirrored on the secondary winding –N • (V_{TRANS} – $V_{DS(ON)}$) which reverse biases the diode and prevents current flow in the secondary winding. Thus, energy is stored in the core of the transformer.

3. Secondary Energy Transfer

When current limit is reached, the current limit comparator resets the NMOS on-latch and the device enters the third phase of operation, secondary energy transfer. The energy stored in the transformer core forward biases the diode and current flows into the output capacitor. During this time, the output voltage (neglecting the diode drop) is reflected back to the primary coil. If the target output voltage is reached, the V_{OUT} comparator resets the master latch and the DONE pin goes low. Otherwise, the device enters the next phase of operation.

4. Discontinuous Mode Detection

Once all the current is transferred to the output capacitor, (V_{OUT} + V_{DIODE})/N will appear across the primary winding. A transformer with no energy cannot support a DC voltage, so, the voltage across the primary will decay to zero. In other words, the drain of the NMOS will ring down from V_{TRANS} + (V_{OUT} + V_{DIODE})/N to V_{TRANS}. When the drain voltage falls to V_{TRANS} + 36mV, the DCM comparator sets the NMOS on-latch and a new charge cycle begins. Steps 2-4 continue until the target output voltage is reached.

APPLICATIONS INFORMATION

Safety Warning

Large capacitors charged to high voltage can deliver a lethal amount of energy if handled improperly. It is particularly important to observe appropriate safety measures when designing the LT3750 into applications. First, create a discharge circuit that allows the designer to safely discharge the output capacitor. Second, adequately space high voltage nodes from adjacent traces to satisfy printed circuit board voltage breakdown requirements. High voltage nodes are the drain of the NMOS, the secondary side of the transformer, and the output.

Transformer Selection

The flyback transformer is critical to proper operation of the LT3750. It must be designed carefully so that it does not cause excessive current or voltage on any pin of the part.

As with all circuits, the LT3750 has finite bandwidth. In order to give the LT3750 sufficient time to detect the output voltage, observe the following restrictions on the primary inductance:

$$L_{PRI} \geq \frac{V_{OUT} \bullet 1\mu s}{N \bullet I_{PK}}$$

otherwise, the LT3750 may overcharge the output.

Linear Technology has worked with several leading magnetic component manufacturers to produce flyback transformers for use with the LT3750. Table 1 summarizes the particular transformer characteristics.

Switching Period

The LT3750 employs an open-loop control scheme causing the switching period to decrease with output voltage. Typical switching frequency is between 100kHz to 300kHz. Figure 3 shows typical switching period in an application with a 3A peak current.

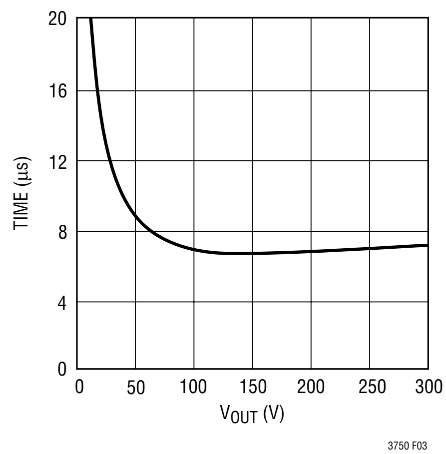


Figure 3. Typical Switching Period vs V_{OUT}

Output Diode Selection

When choosing the rectifying diode, ensure its peak repetitive forward current rating exceeds the peak current (I_{PK}/N) and that the peak repetitive reverse voltage rating exceeds V_{OUT} + (N)(V_{TRANS}). The average current through the diode varies during the charge cycle because the switching period decreases as V_{OUT} increases. The average current through the diode is greatest when the

Table 1. Recommended Transformers

MANUFACTURER	PART NUMBER	SIZE L × W × H (mm)	MAXIMUM I_{PRI} (A)	L_{PRI} (µH)	TURNS RATIO (PRI:SEC)
TDK (www.tdk.com)	DCT15EFD-U44S003	22.5 × 16.5 × 8.5	5	10	1:10
	DCT20EFD-U32S003	30 × 22 × 12	10	10	1:10
Sumida (www.sumida.com)	C8118 Rev P1	21 × 14 × 8	3	10	1:10
	C8117 Rev P1	23 × 18.6 × 10.8	5	10	1:10
	C8119 Rev P1	32.3 × 27 × 14	10	10	1:10
Midcom (www.midcom.com)	32050	23.1 × 18 × 9.4	3	10	1:10
	32051	28.7 × 22 × 11.4	5	10	1:10
	32052	28.7 × 22 × 11.4	10	10	1:10
Coilcraft (www.coilcraft.com)	DA2032-AL	17.2 × 22 × 8.9	3	10	1:10
	DA2033-AL	17.4 × 24.1 × 10.2	5	10	1:10
	DA2034-AL	20.6 × 30 × 11.3	10	10	1:10

APPLICATIONS INFORMATION

output capacitor is almost completely charged and is given by:

$$I_{AVG,D} = \frac{I_{PK} \bullet V_{TRANS}}{2\left(V_{OUT(PK)} + N \bullet V_{TRANS}\right)}$$

The output diode's continuous forward current rating must exceed $I_{AVG,D}$.

At a minimum, the diode must satisfy all the previously mentioned specifications to guarantee proper operation. However, to optimize charge time, reverse recovery time and reverse bias leakage current should be considered. Excessive diode reverse recovery times can cause appreciable discharging of the output capacitor thereby increasing charge time. Choose a diode with a reverse recovery time of less than 100ns. Diode leakage current under high reverse bias bleeds the output capacitor of charge, also increasing charge time. Choose a diode that has minimal reverse bias leakage current. Table 2 recommends several output diodes for various output voltages with adequate reverse recovery time.

Table 2. Recommended Output Diodes

MANUFACTURER	PART NUMBER	I_{DC} (A)	PEAK REPETITIVE REVERSE VOLTAGE (V)	PACKAGE
Diodes Inc. (www.diodes.com)	MURS140	1	400	SMB
	MURS160	1	600	SMB
	ES2G	2	400	SMB
	US1M	1	1000	SMA
Philips (www.semiconductors.philips.com)	BYD147	1	400	SOD87
	BYD167	1	500	SOD87

Bypass Capacitor Selection

Use a high quality X5R or X7R dielectric ceramic capacitor placed close to the LT3750 to locally bypass the V_{CC} and V_{TRANS} pins. For most applications, a 1µF to 10µF ceramic capacitor should suffice for V_{CC} and a 1µF to 10µF for the V_{TRANS} pin.

The high peak currents flowing through the transformer necessitate a larger (>>10µF) capacitor to bypass the primary winding of the transformer. Inadequate bypassing can result in improper operation. This most often manifests itself in two ways. The first is when the primary winding current looks distorted instead of triangular. This substantially reduces the efficiency and increases the charge time. The second way is when the LT3750 fails to detect discontinuous mode after the first switching cycle. Both of these problems are solved by increasing the amount of capacitive bypassing for the transformer. Choose capacitors that can handle the high RMS ripple currents common in flyback regulators.

Output Capacitor Selection

For photoflash applications, the output capacitor will be discharged into a Xenon flash bulb. Only a pulse capacitor or photoflash capacitor is able to survive such a harsh event. Igniting a typical Xenon bulb requires approximately 250V to 350V stored on a capacitor on the order of hundreds of microfarads.

Table 3. Recommended Output Capacitor Vendors

VENDOR	WEBSITE
Rubycon	www.rubycon.com
Cornell Dubilier	www.cornell-dubilier.com
NWL	www.nwl.com

NMOS Selection

Choose an external NMOS with minimal gate charge and on resistance that satisfies current limit and voltage breakdown requirements. The gate is nominally driven to V_{CC} – 2V during each charge cycle. Ensure that this does not exceed the maximum gate to source voltage rating of the NMOS but enhaces the channel enough to minimize the on resistance. Similarly, the maximum drain-source voltage rating of the NMOS must exceed V_{TRANS} + V_{OUT}/N or the magnitude of the leakage inductance spike, whichever is greater. The maximum instantaneous drain current must exceed current limit. Because the switching period decreases with output voltage, the average current through the NMOS is greatest when the output is nearly charged and is given by:

$$I_{AVG,M} = \frac{I_{PK} \bullet V_{OUT(PK)}}{2\left(V_{OUT(PK)} + N \bullet V_{TRANS}\right)}$$

APPLICATIONS INFORMATION

Table 4. Recommended NMOS Transisitors

MANUFACTURER	PART NUMBER	I_D (A)	$V_{DS(MAX)}$ (V)	$V_{GS(MAX)}$ (V)	$R_{DS(ON)}$ (mΩ)	PACKAGE
Philips Semiconductor (www.semiconductors.philips.com)	PHM21NQ15T	22.2	150	20	55	HVSON8
	PHK12NQ10T	11.6	100	20	28	SO-8
	PHT6NQ10Y	6.5	100	20	90	SOT223
	PSMN038-100K	6.3	100	20	38	SO-8
International Rectifier (www.irf.com)	IRF7488	6.3	80	20	29	SO-8
	IRF7493	9.3	80	20	15	SO-8
	IRF6644	10.3	100	20	10.7	DirectFET

The transistor's continuous drain current rating must exceed $I_{AVG,M}$.

Table 4 lists recommended NMOS transistors.

Setting Current Limit

A sense resistor from the SOURCE pin to GND implements current limit. The current limit is nominally $78mV/R_{SENSE}$. The average power dissipation rating of the current sense resistor must exceed:

$$P_{RESISTOR} \geq \frac{I_{PK}^2 \bullet R_{SENSE}}{3}\left(\frac{V_{OUT(PK)}}{V_{OUT(PK)} + N \bullet V_{TRANS}}\right)$$

Additionally, there is approximately a 100ns propagation delay from the time that peak current limit is detected to when the gate transitions to the low state. This delay increases the peak current limit by $(V_{TRANS})(t_{DELAY})/L_{PRI}$.

Setting The Target Output Voltage

The parameters that determine the target output voltage are the resistors R_{VOUT} and R_{BG}, the turns ratio of the transformer (N), and the voltage drop across the output diode (V_{DIODE}). The target output voltage is set according to the following equation:

$$V_{OUT} = \left(1.24V \bullet \frac{R_{VOUT}}{R_{BG}} \bullet N\right) - V_{DIODE}$$

Use at least 1% tolerance resistors for R_{VOUT} and R_{BG}. Choosing large value resistors for R_{BG} decreases the amount of current that charges the parasitic internal capacitances and degrades the response time of the V_{OUT} comparator. This may result in overcharging of the output capacitor. The maximum recommended value for R_{BG} is 2.5k for typical applications.

When high primary currents are used, a voltage spike can prematurely trip the output voltage comparator. A 33pF to 100pF capacitor in parallel with R_{BG} is sufficient to filter this spike for most applications. Always check that the voltage waveform on RBG does not overshoot and that it reaches a plateau at maximum V_{OUT}.

Discontinuous Mode Detection

The R_{DCM} resistor stands off voltage transients on the drain node. A 43k, 5% resistor is recommended for 300V applications. Higher output voltages will require a larger resistor.

In order for the LT3750 to properly detect discontinuous mode and start a new charge cycle, the reflected voltage to the primary winding must exceed the discontinuous mode comparator threshold which is nominally 36mV. The worst-case condition occurs when V_{OUT} is shorted to ground. When this occurs, the reflected voltage is simply the diode forward voltage drop divided by N.

APPLICATIONS INFORMATION

Board Layout

The high voltage operation of the the LT3750 demands careful attention to board layout. Observe the following points:

1. Minimize the area of the high voltage end of the secondary winding.
2. Provide sufficient spacing for all high voltage nodes (NMOS drain, V_{OUT} and the secondary winding of the transformer) in order to meet breakdown voltage requirements.
3. Keep the electrical path formed by C1, the primary of T1 and drain of the NMOS as small as possible. Increasing the size of this path effectively increases the leakage inductance of T1 resulting in an overvoltage condition on the drain of the NMOS.

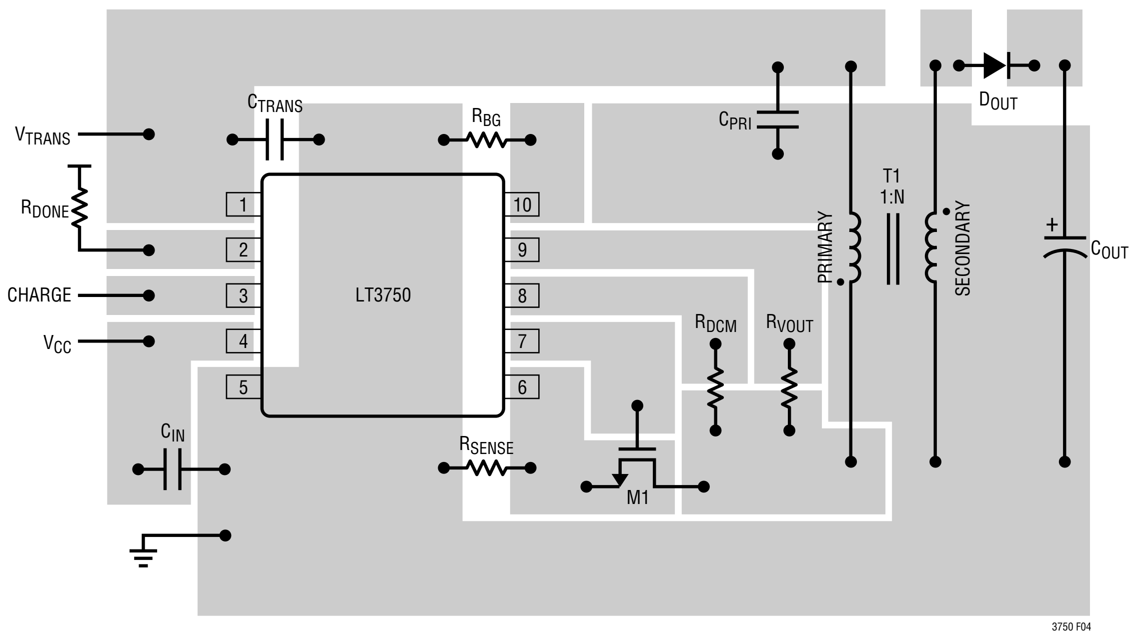
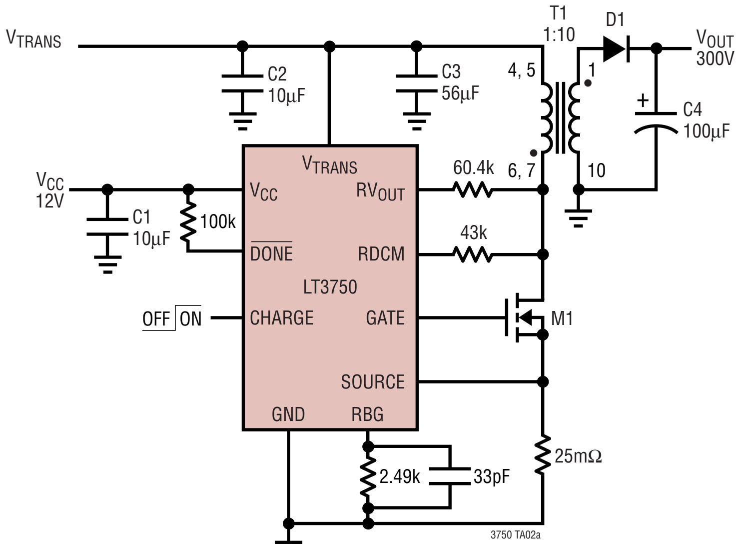


Figure 4. Recommended Board Layout (Not to Scale)

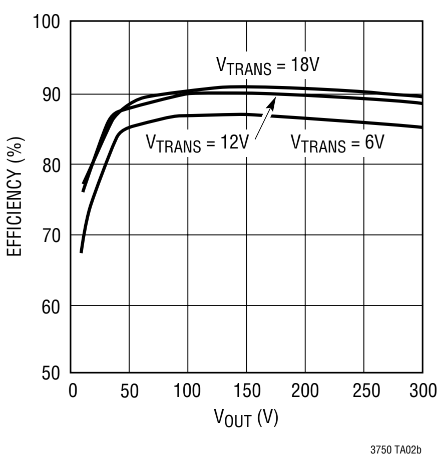
TYPICAL APPLICATIONS

300V, 3A Capacitor Charger

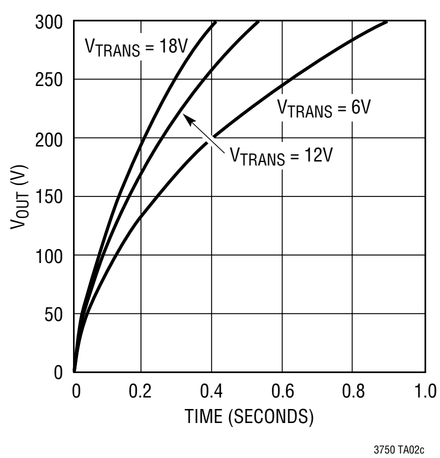


C1: 25V X5R OR X7R CERAMIC CAPACITOR
C2: 25V X5R OR X7R CERAMIC CAPACITOR
C3: 25V SANYO OS-CON 25SVP56M
C4: 330V RUBYCON PHOTOFLASH CAPACITOR
D1: DIODES INC. MURS160
M1: PHILIPS PHT6NQ10T
T1: TDK DCT15EFD-U44S003 FLYBACK TRANSFORMER

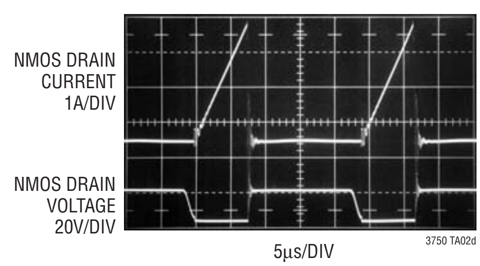
3A Charging Efficiency



3A Charge Time

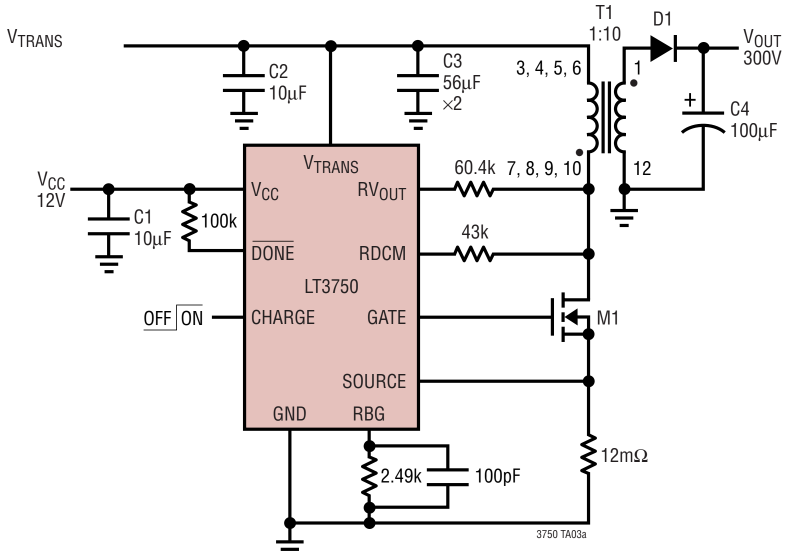


Typical Switching Waveforms



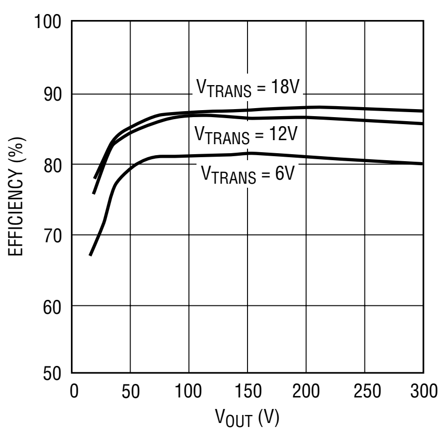
TYPICAL APPLICATIONS

300V, 6A Capacitor Charger

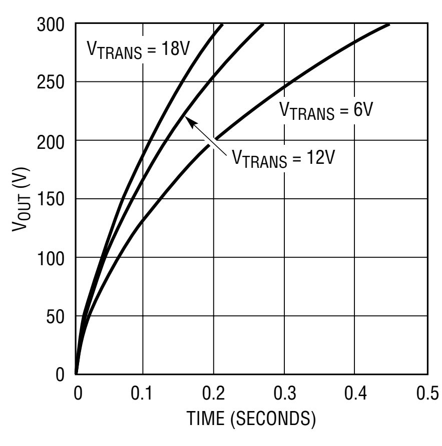


C1: 25V X5R OR X7R CERAMIC CAPACITOR
C2: 25V X5R OR X7R CERAMIC CAPACITOR
C3: 25V SANYO OS-CON 25SVP56M
C4: 330V RUBYCON PHOTOFLASH CAPACITOR
D1: DIODES INC. MURS160
M1: PHILIPS PHT6NQ10T
T1: TDK DCT20EFD-U32S003 FLYBACK TRANSFORMER

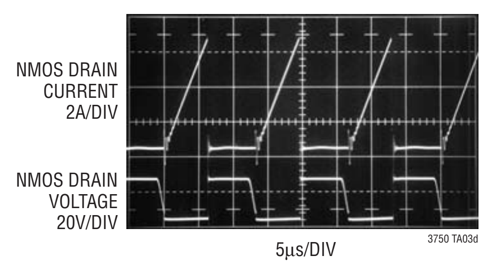
6A Charging Efficiency



6A Charge Time

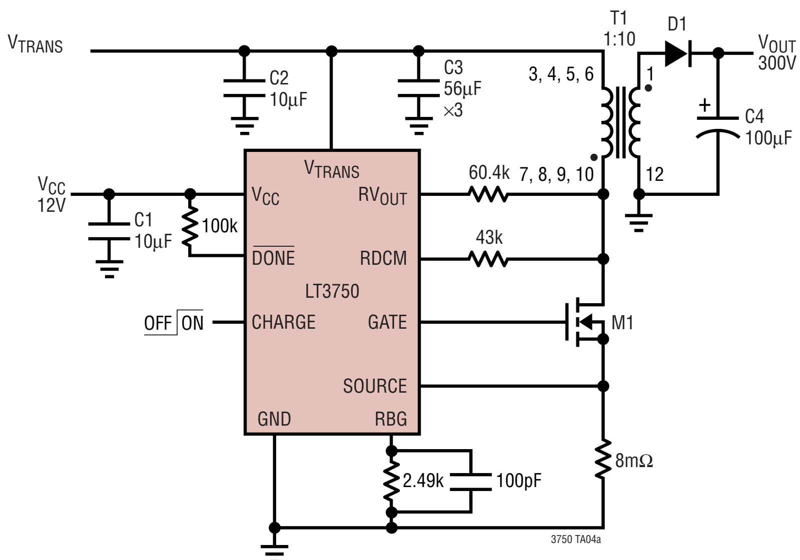


Typical Switching Waveforms



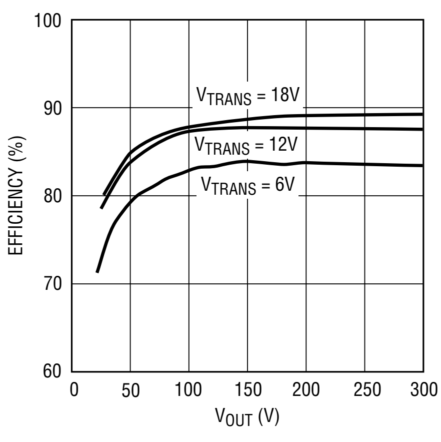
TYPICAL APPLICATIONS

300V, 9A Capacitor Charger

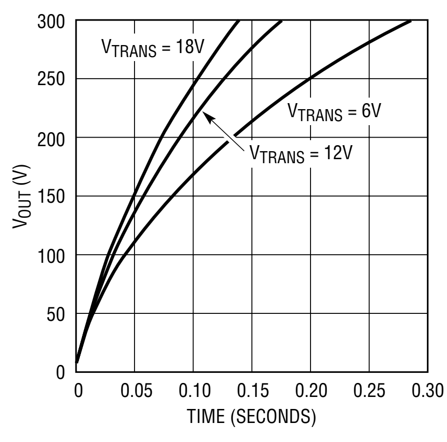


C1: 25V X5R OR X7R CERAMIC CAPACITOR
C2: 25V X5R OR X7R CERAMIC CAPACITOR
C3: 25V SANYO OS-CON 25SVP56M
C4: 330V RUBYCON PHOTOFLASH CAPACITOR
D1: DIODES INC. MURS160
M1: PHILIPS PHM2INQ15T
T1: TDK DCT20EFD-U32S003 FLYBACK TRANSFORMER

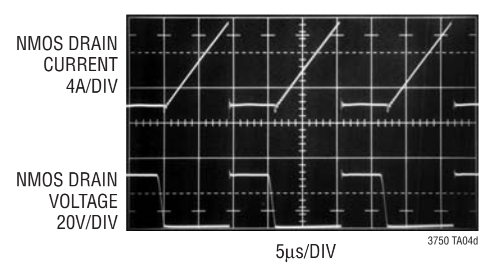
9A Charging Efficiency



9A Charge Time

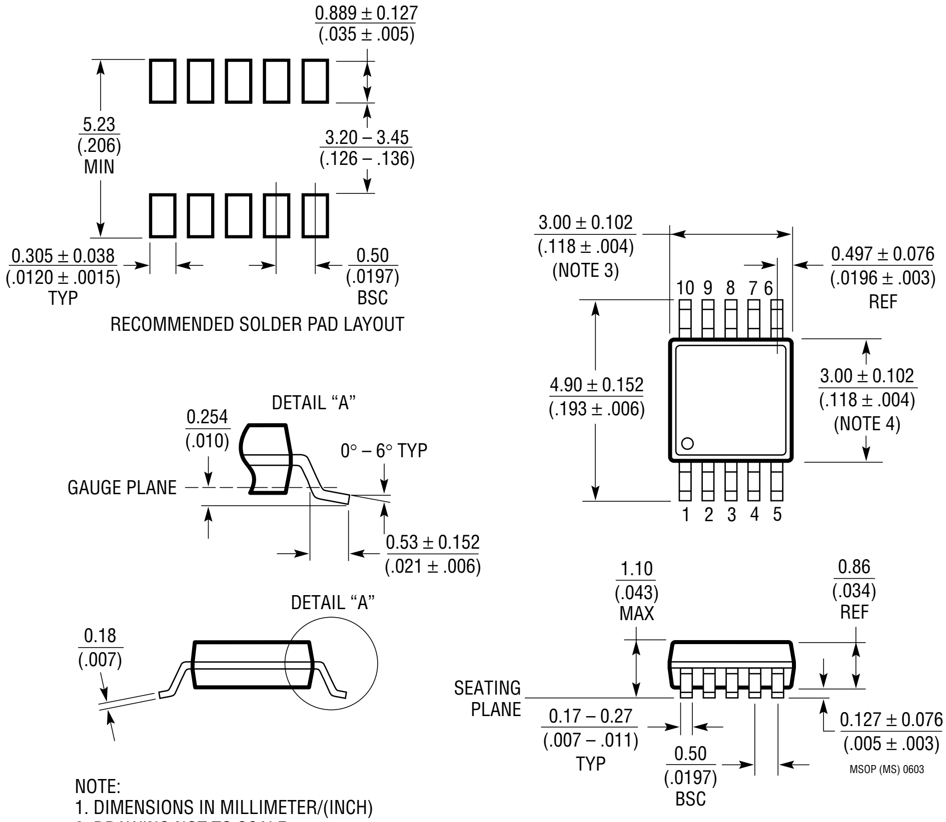


Typical Switching Waveforms



PACKAGE DESCRIPTION

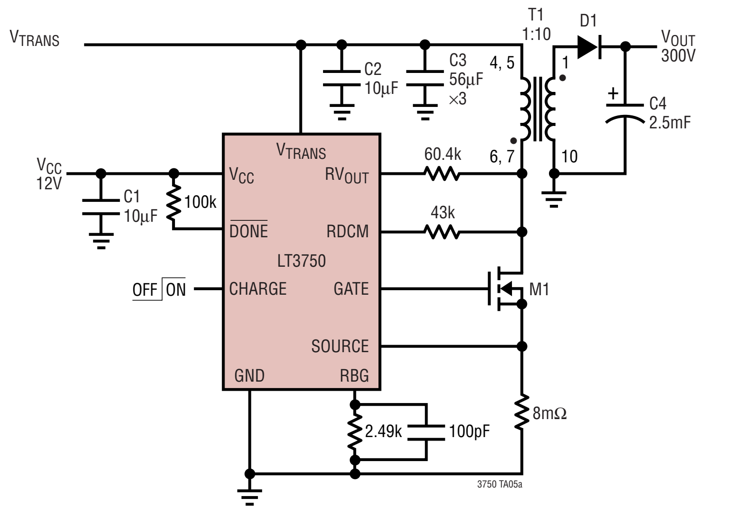
MS Package
10-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1661)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

TYPICAL APPLICATION

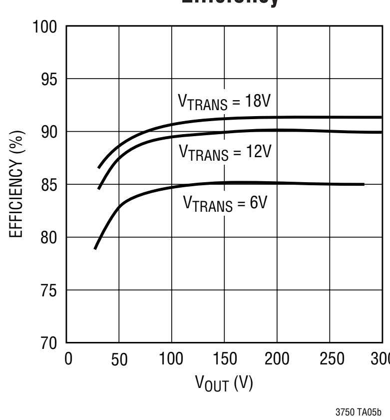
300V, 9A, 2.5mF Capacitor Charger



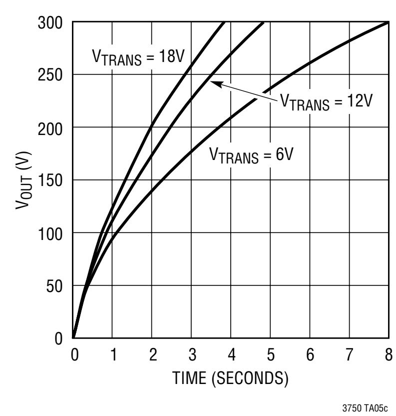
C1, C2: 25V X5R OR X7R CERAMIC CAPACITOR
C3: 25V SANYO OS-CON 25SVP56M
C4: CORNELL DUBILIER 7P252V360N082

D1: DIODES INC. MURS160
M1: PHILIPS PHM21NQ15T
T1: MIDCOM 32052 FLYBACK TRANSFORMER

Efficiency



Charge Time



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT3420/LT3420-1	1.4A/1A, Photoflash Capacitor Charger with Automatic Top-Off	Charges 220µF to 320V in 3.7 Seconds from 5V, V_{IN}: 2.2V to 16V, I_{SD} < 1µA, 10-Lead MS Package
LT3468/LT3468-1 LT3468-2	1.4A, 1A, 0.7A, Photoflash Capacitor Charger	V_{IN}: 2.5V to 16V, Charge Time: 4.6 Seconds for LT3468 (0V to 320V, 100µF, V_{IN} = 3.6V), I_{SD} < 1µA, ThinSOT Package
LT3484-0/LT3484-1 LT3484-2	1.4A, 0.7A, 1A Photoflash Capacitor Charger	V_{IN}: 1.8V to 16V, Charge Time: 4.6 Seconds for LT3484-0 (0V to 320V, 100µF, V_{IN} = 3.6V), I_{SD} < 1µA, 2mm × 3mm 6-Lead DFN Package
LT3485-0/LT3485-1 LT3485-2/LT3485-3	1.4A, 0.7A, 1A, 2A Photoflash Capacitor Charger with Output Voltage Monitor and Integrated IGBT Driver	V_{IN}: 1.8V to 10V, Charge Time: 3.7 Seconds for LT3485-0 (0V to 320V, 100µF, V_{IN} = 3.6V), I_{SD} < 1µA, 3mm × 3mm 10-Lead DFN

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